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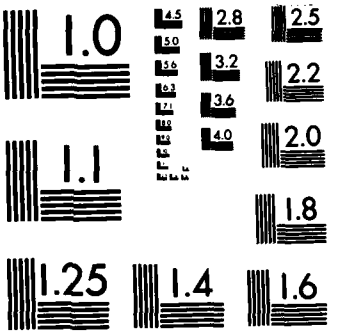

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George Lewicki

Prototyping and Small-Volume Parts through MOSIS

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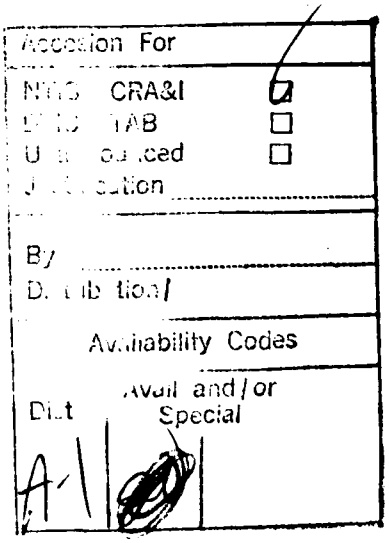

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Prototyping and Small-Volume Parts through MOSIS

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Introduction

Since 1980, the Information Sciences Institute of the University of Southern California has been managing the MOS Implementation System (MOSIS) for DARPA's VLSI design research community. MOSIS allows designers to easily obtain both prototype and small-volume production quantities of custom integrated circuit parts. Designers send MOSIS their integrated circuit geometry, designed against a process specification and a set of design rules. MOSIS buys wafers against this process specification, has parts assembled, and ships the packaged parts to their designer. MOSIS maintains a vendor base of at least three fabricators for each technology. The designer assumes responsibility for his circuit being functional; MOSIS assures that the process specification has been met and that defect densities are within normal limits.

In order to satisfy the quality assurance requirements of some of the members of its design community, MOSIS is developing a quality assurance methodology which takes advantage of its regular access to wafers (as opposed to packaged parts).

MOSIS currently handles approximately 1600 design projects per year for over 100 separate organizations. All communication between MOSIS and its design community is conducted over the ARPANET, a government-sponsored computer communications network .

This paper describes the interrelated activities carried out by designers, MOSIS, and fabricators to generate custom integrated circuit parts. The various MOSIS-supported technologies are listed, and a plan for MOSIS to develop a quality assurance methodology is discussed.

Activities in the Acquisition of Parts through MOSIS

The designer, the U.S. semiconductor industry, and MOSIS all play roles in the acquisition of parts, as outlined below.

1. MOSIS: Defines a process specification and a set of design rules for each technology. This definition is based on a survey of the industry to determine those rules and specifications which can support a large segment of the fabricator community.

   MOSIS: Distributes those rules and specifications to its design community over the ARPANET.

2. DESIGNER: Designs against those rules and specifications. The designs are submitted to MOSIS in CIF (Caltech Intermediate Form) or CALMA GDS2 Stream Format. The tools used to generate these designs are not provided by MOSIS.

   Acquisition and proper use of design tools is considered the responsibility of the user, who typically obtains them from either commercial CAD vendors or from universities.

3. MOSIS: Serves as the design community's librarian. MOSIS has always provided pads for each of the technologies being supported. It is now expanding its role as a librarian by a) making available and maintaining a government-developed 3-micron p-well CMOS/Bulk standard cell library; b) assisting CAD vendors in installing this library into their systems; and c) making available and maintaining verified, higher level functional blocks (such as RAMS, ROMS, register stacks, and data paths), which have been submitted to MOSIS by members of its design community .

4. MOSIS: Schedules fabrication runs in each technology on a regular basis, and publishes this schedule approximately six months in advance.

   These prototyping runs allow users to develop their designs and to determine yield with each of the fabricators in the vendor base. The runs carry a large number of users (typically about 40). Users are provided with a small quantity of parts in order to verify their designs and determine yield. MOSIS uses processes capable of using

full-wafer lithography, and mask makers with E-beam equipment that is easily capable of putting a large number of different die types onto a single set of masks. When a run is shared by many users, the cost of the run is also shared.

5. MOSIS: Holds small-volume production runs for those designers who need larger quantities of parts. Designers must first successfully develop their designs and determine yield in prototyping runs. These runs are initiated on request and typically serve from one to three users.

6. MOSIS: Places geometry on the wafer and does all the necessary transformations on both the users' and the wafer fabricators' geometry to generate the tapes that drive the mask makers' equipment.

MOSIS goes to considerable effort to have its phototooling indistinguishable from that of the fabricator. The fabricators' process control monitor (PCM), alignment marks, etc., are provided at locations specified by the fabricators.

7. INDUSTRY: Processes the required phototooling using E-beam equipment.

8. INDUSTRY: Fabricates wafers using phototooling provided by MOSIS.

9. MOSIS: Accepts or rejects wafers. Wafers are accepted on the basis of the process specifications having been met, as evidenced by the fabricators' measurements on their own PCMs and MOSIS' measurements on its PCM. Functionality of users' circuits is not an acceptance criterion.

All measurements made by MOSIS on each run's PCM are reported to the designers. Parameters measured include sheet resistances, contact resistances, process constants, capacitances, and transistor characteristics. SPICE decks containing values for SPICE parameters giving best fits for measured transistor characteristics are also distributed to the community.

MOSIS, in conjunction with a number of interested parties, is developing a quality assurance methodology based not only on a vendor's control of his process as evidenced by measurements on a

PCM, but also on a) the degree of existence of various failure mechanisms such as time-dependent breakdown, contact electro-migration, etc., as evidenced by measurements on specialized test structures; and b) failure rates experienced during accelerated testing of "canaries" representing particular styles of design. When that methodology is developed, MOSIS will be able to accept and screen wafers on the basis of their quality as well as their parameters.

10. MOSIS: Performs wafer-level functional screening of parts in small-volume production runs.

Before doing such a run, MOSIS requires that the user submit both a working part and test code in a very simple MOSIS-supported test language known as SIEVE. The part and the code are used to verify that MOSIS' tester can correctly interpret the test language. The code is then used to functionally screen parts at wafer level, solely for the purpose of reducing the packaging of bad parts.

11. INDUSTRY: Provides assembly per instructions provided by MOSIS.

12. INDUSTRY: Provides burn-in and accelerated testing when required.

13. MOSIS: Distributes untested packaged parts and run-specific parametric data.

14. DESIGNER: Tests prototype parts for functionality, speed, and yield. Submits a report to MOSIS.

Technologies Supported by MOSIS

The current MOSIS-supported technologies are as follows:

1. *nMOS 3- and 4-microns:* The design rules for this technology are essentially those described in the Mead/Conway text, *Introduction to VLSI Design*. The only difference is the replacement of a butting contact rule by a buried contact rule to accommodate fabricators' transitions from wet to dry etching. It is interesting to note that the Mead/Conway scalable rules were applicable to the 5-micron feature size processes commonly available in 1979 and remain applicable to the 3-micron feature size processes available now.

MOSIS nMOS prototyping runs are scheduled every three weeks.

2. *CMOS/Bulk 3-microns, p-well:* The design rules and process specifications adopted for this technology were those defined by a large government agency for the design of a standard cell library to be used in their design of semi-custom parts to be fabricated by industry. MOSIS is making this library available to its user community, which is submitting for fabrication both full-custom and library-based designs.

The frequency of prototyping runs in this technology is currently one run every three weeks.

3. *CMOS/Bulk 1.2-microns:* MOSIS is distributing to its community a set of generic and scalable CMOS/Bulk design rules applicable to p-well, n-well, and twin-tub processes with feature sizes of 3-, 2-, and 1.2-microns. The scalable rules were specifically optimized for 1.2-micron processes; they are not as aggressive at 3-microns as those specifically designed for 3-micron p-well processes.

MOSIS has carried out four experimental runs at 1.2-microns and is planning to make this technology available to its community towards the end of 1986.

One feature of the 1.2-micron technology is that it is stepper-based, and MOSIS must provide its fabricators 10x or 5x reticles rather than 1x full-wafer masks. The result is that 1.2-micron runs cannot be shared among users to anywhere near the extent possible with the full-wafer lithography processes which can be used with a larger feature size.

To minimize costs, MOSIS is proposing that its community do the initial design development at the smallest feature size full-wafer lithography processes available to MOSIS, before going on to 1.2-micron fabrication. MOSIS' scalable CMOS design rules facilitate this approach. The smallest feature size full-wafer lithography process currently available to MOSIS is 3-micron p-well CMOS.

4. *CMOS/Bulk 2- and 3-microns, p- and n-well:* MOSIS is currently arranging for experimental runs with various fabricators to determine the viability of its scalable rules with processes other than 3-micron p-well. When appropriate, MOSIS will make these processes available to its community.

5. *CMOS/SOS 4-microns:* There is a small segment of the MOSIS university community teaching SOS design. MOSIS arranges runs for this technology approximately twice a year.

6. *Printed Circuit Boards (PCBs):* MOSIS maintains a base of PCB manufacturers and accepts PCB geometry in CIF. There are no run schedules associated with PCBs -- manufacture is initiated on receipt of geometry. MOSIS also can work with manufacturers capable of fabricating from parts and net lists.

There is no shared-cost benefit in obtaining PCBs through MOSIS, as each PCB is dedicated to a single designer. MOSIS treats PCB fabrication as yet another technology, with its own set of conventions, standard cells, and geometric and electric design rules. The geometric processing required to convert CIF into tooling for PCBs is similar to that required for any other technology.

MOSIS Quality Assurance Plans

A significant fraction of the MOSIS design community requires small-volume numbers of custom parts with predictable failure rates. MOSIS is planning to develop a quality assurance methodology that would allow such predictions to be made. The first technology addressed will be 3-micron CMOS/Bulk p-well, because the MOSIS-supported standard cell library is based on that technology and the majority of MOSIS users interested in quality assurance are users of the MOSIS-supported standard cell library.

MOSIS plans to correlate failure rates experienced during burn-in and accelerated testing of a standard-cell-based circuit to results obtained from wafer-level measurements of

- a fabricator's control over his process using MOSIS' PCM, and
- the degree of existence of silicon-related wearout mechanisms (such as time-dependent breakdown, gate oxide instabilities, and contact electromigration utilizing specialized test structures).

At best, establishment of such a correlation will allow easier wafer-level measurements on test structures to predict failure rates of parts from the same wafer. At worst, the correlation should allow wafer-level measurements to act as a screen for parts to be put through burn-in and accelerated testing, which would then be used to predict failure rates.

The scope of the correlation effort will be on the order of ten CMOS/Bulk 3-micron, p-well runs. Fully automated test equipment will be used to make wafer-level measurements on MOSIS' PCM and on a reliability test structure. Industry will be contracted to do the burn-in and accelerated testing.

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